WHAT IS CLAIMED IS:

1. A resistance-changing function body comprising:

a first electrode;

a second electrode;

a medium made of a first material interposed between the first electrode and the second electrode; and

at least one conductive particle made of a third material, having a surface covered with a second material and included in the medium, wherein

the second material has a barrier against passage of electric charges,

the third material has a capability to retain electric charges, and

an electrical resistance between the first electrode and the second electrode is changed depending on an amount of electric charges accumulated in the particle.

2. The resistance-changing function body as claimed in claim 1, wherein

the first material and the second material are mutually different insulative substances,

the third material is a conductive material, and

the second material is an insulative substance formed by using the third material.

3. A memory element comprising:

a first electrode;

a second electrode; and

a memory function body interposed between the first electrode and the second electrode, wherein

the memory function body includes:

a first insulator; and

a conductive particle included in the first insulator and having a surface covered with a material having a barrier against passage of electric charges, and wherein

a magnitude of a current through the memory function body changes by application of a prescribed voltage between the first electrode and the second electrode, and a storage state is discriminated according to the magnitude of the current.

4. A memory device comprising a memory cell including:

the memory element as claimed in claim 3; and

a rectifying function body having a rectification effect so as to determine a direction of the current through the memory function body of the memory element, wherein

the memory element and the rectifying function body are electrically connected in series to each other.

5. A memory device comprising a memory cell including:

the memory element as claimed in claim 3; and

a select transistor for selecting the memory element, wherein

the memory element and the select transistor are electrically connected in series to each other.

6. A memory device comprising at least two memory cells each including the memory element as claimed in claim 3, wherein

the first insulators of the memory function bodies of the two memory cells are integrally continuously formed, and

the first electrode of one memory cell of the two memory cells and the first electrode of the other memory cell are electrically connected to each other, and the second electrode of the one memory cell and the second electrode of the other memory cell are electrically isolated from each other.

7. A memory device comprising:

at least five memory cells each including the memory element as claimed in claim 3;

bit lines extended in a direction of column;

source lines extended in a direction of column; and

word lines extended in a direction of row, wherein

each of the memory cells includes:

a select transistor for selecting the memory element; and

a rectifying function body for determining a direction of the current through the memory function body of the memory element, and wherein

each of the memory cells is connected between the bit line and the source line, and the select transistor of each of the memory cells is controlled by the word line,

with respect to a first memory cell of the five memory cells, a second and a fourth memory cells are arranged mutually adjacently in the direction of row, and a third and a fifth memory cells are arranged mutually adjacently in the direction of column,

the first memory cell and the second memory cell have a shared bit line, a shared word line and an unshared source line,

the first memory cell and the third memory cell have a shared bit line, a shared source line and an unshared word line,

the first memory cell and the fourth memory cell have a shared source line, a shared word line and an unshared bit line,

the first memory cell and the fifth memory cell have a shared word line,

a source line of the first memory cell and a bit line of the fifth memory cell are shared, and

a bit line of the first memory cell and a source line of the fifth memory cell are shared.

8. The memory device as claimed in claim 7, wherein

at least two memory cells are arranged in a direction parallel to a substrate, and

the first insulators of the memory function bodies of the memory cells mutually adjacent in the direction parallel to the substrate are integrally continuously formed.

9. The memory device as claimed in claim 7, wherein

at least two memory cells are arranged in a direction parallel to a substrate, and

the first insulators and/or the rectifying function bodies of the memory cells mutually adjacent in the direction parallel to the substrate are integrally continuously formed.

10. The memory element as claimed in claim 3, further comprising

a third electrode adjacent to the memory function body, wherein

the third electrode is able to apply a voltage to the memory function body in a position between the first electrode and the second electrode in a direction opposing the first electrode and the second electrode to each other.

11. The memory element as claimed in claim 10, wherein

the first electrode and the second electrode are each formed on a surface of a semiconductor substrate,

the memory function body is formed in a region located between the electrodes on the surface of the semiconductor substrate, and

the third electrode is provided on the memory function body.

12. The memory element as claimed in claim 10, wherein

the first electrode and the second electrode are each made of a conductor formed on a substrate,

the memory function body is formed in a region interposed between the conductors, and

the third electrode is provided on the memory function body.

13. A memory device comprising:

at least two memory cells each including the memory element as claimed in claim 3, wherein

the memory cells are formed on a substrate, and

the memory function bodies of the memory cells are laminated in a direction perpendicular to the substrate.

14. A method for manufacturing the memory element claimed in claim 3, comprising the step of:

implanting a substance for forming the conductive particle in the first insulator by a negative ion implantation method.

15. A semiconductor device comprising the memory element claimed in claim 3.

16. Electronic equipment comprising the semiconductor device claimed in claim 15.